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Chapter 1 Exercise Solutions. VLSI Test Principles and Architectures Ch. 1 - Introduction - P. 1/2. Chapter 1 Exercise

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Solutions. 1.1. There are 14 nodes in the circuit. Thus, there are $14 \times 2 = 28$ single stuck-at faults. For multiple stuck-at fault, it has $(2 + 1)14 - 1 = 4782968$ multiple stuck-at faults.

Chapter 1 Exercise Solutions

VLSI Test Principles and Architectures Ch. 6 - Test Compression - P. 1/3 Chapter 6 Exercise Solutions: 6.1 The complete dictionary at least includes the following five entries: 0000 0110 0100 0001 1100. The five 4-bit entries can be encoded into five 3-bit entries. The compression ratio is: $(1-3/4) * 100\% = 25\%$. 6.2

Chapter 6 Exercise Solutions - IC-Test Lab, NCUE, Taiwan

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VLSI Test Principles and Architectures Ch. 2 - Design for Testability - P. 5/12 2.10 (Full-Scan Design) 1. In an LSSD single-latch design, the output of the master latch L1 is used to drive combinational logic, and the slave latch L2 is used for scan shift. While in an LSSD double-latch design, the

Chapter 2 Exercise Solutions 2.1 Testability Analysis

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